

Universitatea Transilvania din Braşov

Facultatea IESC

Departamentul EC

Poz. Postului: 32.

Disciplinele postului:

Sisteme cu microprocesoare

Sisteme electronice încorporate

Microcontrolere

Microprocesoare şi microcontrolere

Sisteme dedicate pe bază de calculator (Embedded Systems)

FIŞA DE VERIFICARE A ÎNDEPLINIRII STANDARDELOR UNIVERSITĂŢII

Postul: Şef lucrări (pe perioadă determinată), poziţia 32,
publicat în Monitorul Oficial al României¹ nr. din data de

Candidat: Cătălin Bogdan Ciobanu Data naşterii 13.04.1983

Funcţia actuală: Cadru didactic asociat Instituţia Universitatea Transilvania Braşov

1. Studii universitare (licenţă şi masterat)

Nr. crt.	Instituţia de învăţământ superior şi facultatea	Domeniul	Perioada	Titlul acordat
1	Universitatea Transilvania Braşov, Facultatea de Inginerie Electrică şi Ştiinţa Calculatoarelor	Profilul Electronic, specializarea Electronică Aplicată	2001-2006	Inginer Diplomat
2	Technische Universiteit Delft, Olanda, Faculty of Electrical Engineering, Mathematics and Computer Science	Computer Engineering	2006-2007	Master of Science

2. Studii de doctorat

Nr. crt.	Instituţia organizatoare de doctorat	Domeniul	Perioada	Titlul ştiinţific acordat
1	Technische Universiteit Delft, Olanda	Computer Engineering	2007-2013	Doctor

3. Studii şi burse postdoctorale (stagii de cel puţin 6 luni)

Nr. crt.	Instituţia	Domeniul/ Specializarea	Perioada	Tipul de bursă
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¹ Se completează numai în cazul posturilor pe perioadă nedeterminată.

1	Chalmers University of Technology, Suedia	Computer Engineering	2013- 2015	Contract pe proiect european
2	University of Amsterdam, Olanda	Systems and Networking (SNE) lab, Informatics Institute	2015- 2018	Contract pe proiect european

4. Standarde minimale ale universității

Post didactic (se menține în tabel numai postul pentru care se candidează)	Realizări conform standardelor proprii ale Universității
Șef de lucrări	<p>(i) Articol în revistă cotate ISI WoS cu SRI > 0.5, ca prim autor</p> <p>C.B. Ciobanu, G. Gaydadjiev, C. Pilato and D. Sciuto, The Case for Polymorphic Registers in Dataflow Computing, International Journal of Parallel Programming, December 2018, pp. 1185-1219, https://doi.org/10.1007/s10766-017-0494-1</p> <p>Online: https://link.springer.com/article/10.1007/s10766-017-0494-1</p> <p>SRI: 0.608</p> <p>(ii) Alte articole ISI WoS cu SRI > 0.5</p> <p>1. A. L. Machidon, O. M. Machidon, C. B. Ciobanu, and P. L. Ogrutan, "Accelerating a Geometrical Approximated PCA Algorithm Using AVX2 and CUDA," Remote Sensing, vol. 12, no. 12, p. 1918, Jun. 2020 https://doi.org/10.3390/rs12121918</p> <p>Online: https://www.mdpi.com/2072-4292/12/12/1918/htm</p> <p>SRI: 4.509 (2019) ; 5-Year Impact Factor: 5.001 (2019)</p> <p>2. G. Stramondo, C.B. Ciobanu, C. de Laat, A.L. Varbanescu, Designing and Building ApplicationCentric Parallel Memories, in Concurrency and Computation: Practice and Experience, https://doi.org/10.1002/cpe.5485</p> <p>Online: https://onlinelibrary.wiley.com/doi/full/10.1002/cpe.5485</p> <p>SRI: 1.447 (2019), 1.268 (5 year)</p>

(VLSI SoC), pp. 143-148, Verona, Italy, October 2018

3. G. Stramondo, **C. B. Ciobanu**, A. L. Varbanescu, C. de Laat, Towards Application-Centric Parallel Memories, Euro-Par 2018: Parallel Processing Workshops, pp. 481-493, Turin, Italy, August 2018
4. **C. B. Ciobanu**, G. Stramondo, A. L. Varbanescu, A. Brokalakis, A. Nikitakis, L. Di Tucci, M. Rabozzi, L. Stornaiuolo, M. Santambrogio, G. Chrysos, C. Vatsolakis, C. Georgios, and D. Pnevmatikatos, EXTRA: An Open Platform for Reconfigurable Architectures, 2018 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS XVIII), pp. 220-229, Samos Island, Greece, July 2018, <https://doi.acm.org/10.1145/3229631.3236092>
5. **C. B. Ciobanu**, G. Stramondo, C. de Laat and A. L. Varbanescu, MAX-PolyMem: High-Bandwidth Polymorphic Parallel Memories for DFEs, 2018 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), pp. 107-114, Vancouver, Canada, May 2018, <https://doi.org/10.1109/IPDPSW.2018.00025>
6. Kulkarni, P. Bahrebar, D. Stroobandt, G. Stramondo, **C. B. Ciobanu** and A. L. Varbanescu, A NoC-based Custom FPGA Configuration Memory Architecture for Ultra-fast Micro-reconfiguration, 2017 International Conference on Field Programmable Technology (ICFPT), pp. 203-206, Melbourne, Australia, December 2017

Luk, M. D. Santambrogio, D. Sciuto, M. A. Kadi, M. Huebner, T. Becker, and G. Gaydadjiev, A. Brokalakis, A. Nikitakis, A. J. W. Thom, E. Vansteenkiste, D. Stroobandt, EXTRA: Towards an Efficient Open Platform for Reconfigurable High Performance Computing, 2015 IEEE 18th International Conference on Computational Science and Engineering, pp. 339-342, Porto, Portugal, October 2015

12. G. Smaragdous, C. Davies, C. Strydis, I. Sourdis, C.B. Ciobanu, O. Mencer, C. De Zeeuw, Real-Time Olivary Neuron Simulations on Dataflow Computing Machines, Proceedings of International Supercomputing Conference (ISC 2014), pp. 487-497, Leipzig, Germany, June 2014
13. C.B. Ciobanu, G.N. Gaydadjiev, C. Pilato, D. Sciuto, Dataflow Computing with Polymorphic Registers, Proceedings of the 2013 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS 2013), pp. 314-321, Samos, Greece, July 2013
14. C.B. Ciobanu, D.N. Pnevmatikatos, K.D. Papadimitriou, G.N. Gaydadjiev, FASTER Runtime Reconfiguration Management, Proceedings of the 27th International Conference on Supercomputing (ICS 2013), pp. 463-464, Eugene, Oregon, USA, June 2013
15. C.B. Ciobanu, G. N. Gaydadjiev, Separable 2d Convolution with Polymorphic Register Files, Proceedings of the 2013 Conference on Architecture of Computing Systems (ARCS 2013), pp. 317-328, Prague, Czech Republic, February 2013

16. K. Papadimitriou, C. Pilato, D. Pnevmatikatos, M.D. Santambrogio, C.B. Ciobanu, T. Todman, T. Becker, T. Davidson, X. Niu, G. N. Gaydadjiev, W. Luk, D. Stroobandt, Novel Design Methods and a Tool Flow for Unleashing Dynamic Reconfiguration, Proceedings of the 15 th International Conference on Computational Science and Engineering (CSE 2012), pp. 391-398, December 2012
17. C.B. Ciobanu, G. Kuzmanov, G. N. Gaydadjiev, Scalability Study of Polymorphic Register Files, Proceedings of the international conference on Digital System Design (DSD 2012), pp. 803-808, Cesme, Izmir, Turkey, September 2012
18. C.B. Ciobanu, G. Kuzmanov, G. N. Gaydadjiev, On Implementability of Polymorphic Register Files, Proceedings of the 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC 2012), pp. 1-6, York, UK, July 2012
19. C. B. Ciobanu, G. Kuzmanov, A. Ramirez, G. N. Gaydadjiev, Parallel Access Schemes for Polymorphic Register Files: Motivation Study, Advanced Computer Architecture and Compilation for Embedded Systems (ACACES), pp. 127-130, Fiuggi, Italy, 2011
20. C. B. Ciobanu, X. Martorell, G. Kuzmanov, A. Ramirez, G. N. Gaydadjiev, Scalability Evaluation of a Polymorphic Register File: a CG Case Study, Proceedings of the 2011 Conference on Architecture of Computing Systems (ARCS 2011), pp. 13-25, Como, Italy, 2011

21. C. B. Ciobanu, G. Kuzmanov, A. Ramirez, G. N. Gaydadjiev, A Polymorphic Register File for Matrix Operations, Proceedings of the 2010 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS 2010), pp. 241-249, Samos, Greece, 2010
22. C. B. Ciobanu, G. Kuzmanov, A. Ramirez, G. N. Gaydadjiev, A Polymorphic Register File Architecture, Advanced Computer Architecture and Compilation for Embedded Systems (ACACES), pp. 245-248, Terrassa, Spain, 2009
23. D. Theodoropoulos, C. B. Ciobanu, G. Kuzmanov, Wave Field Synthesis for 3D Audio: Architectural Perspectives, ACM International Conference on Computing Frontiers, pp. 127-136, Ischia, Italy, 2009
24. B. Spinean, C. B. Ciobanu, G. Kuzmanov, G. N. Gaydadjiev, Design Considerations for a Domain Specific Vector Microarchitecture, in proceedings of PRORISC 2007, pp. pp. 178-184, Veldhoven, The Netherlands, 2007
25. C. B. Ciobanu, B. Spinean, G. Kuzmanov, G. N. Gaydadjiev, Customized Vector Instruction Set Architecture, proceedings of PRORISC 2007, pp. 128-137, Veldhoven, The Netherlands, 2007

(iv) Volum(e) de specialitate publicat(e) în edituri recunoscute național

1. C.B. Ciobanu, Customizable Register Files for Multidimensional SIMD architectures, Delft University of Technology, 2013, ISBN 978-94-6186-121-4

	<p>2. L. Stornaiuolo, M. Rabozzi, M. D. Santambrogio, D. Sciuto, C. B. Ciobanu, G. Stramondo, A. L. Varbanescu, Building High-Performance, Easy-to-Use Polymorphic Parallel Memories with HLS, capitol în VLSI-SoC: Design and Engineering of Electronics Systems Based on New Computing Paradigms, Springer, Cham, 2019, ISBN 978-3-030-23424-9</p> <p>3. C.B. Ciobanu, Embedded Systems - Îndrumar de Proiect, în curs de publicare, Editura Universității Transilvania Brașov, 2020</p> <p>(v) Media anilor studii licență: 9.52</p>

Candidat,

Rezoluția Comisiei științifice:

Membrii Comisiei științifice:

1. prof. dr. MIHAI IVANOVICI
2. prof. dr. FLORIN MOLDOVEANU
3. prof. dr. DORU URSUTIU

Standardele sunt îndeplinite:

<input checked="" type="checkbox"/> Da	<input type="checkbox"/> Nu
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<input checked="" type="checkbox"/> Da	<input type="checkbox"/> Nu

DA D. Ursutiu

Sir. DEC

[Signature]