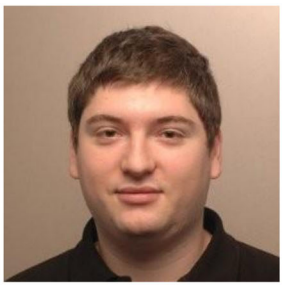
INFORMAŢII PERSONALE

Cătălin Bogdan CIOBANU



Brașov, România

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Data naşterii | Naţionalitatea Română

EXPERIENŢA PROFESIONALĂ

Oct 2020 – prezent	**Șef de Lucrări**, **Universitatea Transilvania din Brașov**, Facultatea de Inginerie Electrică și Știința Calculatoarelor
Oct 2019 – Sep 2020	**Cadru didactic asociat, Universitatea Transilvania din Brașov**, Facultatea de Inginerie Electrică și Știința Calculatoarelor
Apr 2020 – Mar 2021	**High-Performance Data Engineer, Niometrics**, Brașov, România
Sep 2018 – Sep 2020	**Cercetător, Delft University of Technology**, Olanda
Oct 2015 – Aug 2018	**Cercetător, University of Amsterdam**, Olanda Proiectul European EU2020 EXTRA (Exploiting eXascale Technology with Reconfigurable Architectures)
Mai 2015 – Sep 2015	**Cercetător PostDoctoral, Delft University of Technology**, Olanda
Mao 2013 – Apr 2015	**Cercetător PostDoctoral, Chalmers University of Technology**, Suedia FASTER (“Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration”) project
Apr 2012 – Apr 2013	**Asistent de Proiect, Chalmers University of Technology**, Suedia Proiectul European FP7 FASTER (“Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration”)
	Asistent didactic, Delft University of Technology, Olanda
Sep 2010 - Noi 2010, Sep 2009 - Noi 2009 Mar 2009	System Programming in C Computer Systems
Apr 2008 - Iun 2008, Apr 2007 - Iun 2007 Sep 2008 - Noi 2008, Sep 2007 - Noi 2007	Programming with C++ Java and Object-Oriented Design
Mar 2005 – Aug 2005	**Siemens Program and System Engineering**, Brașov, România
Sep 2003 – Aug 2005	**UTI Grup**, Brașov, România

EDUCAŢIE ŞI FORMARE

Apr 2007 – Mar 2013	**Doctorat**, Ingineria Calculatoarelor **Delft University of Technology**, Olanda **Proiect**: Scalable computer ARChitecture (SARC) **Teza**: Customizable Register Files for Multidimensional SIMD Architectures
Sep 2005 – Apr 2007	**Master**, Ingineria Calculatoarelor **Delft University of Technology**, Olanda **Teza:** “Customized Vector Instruction Set Architecture”
Sep 2001 – Aug 2006	**Diplomă de inginer** Inginerie Electrică și Știința Calculatoarelor, profilul Electronic, specializarea Electronică Aplicată **Universitatea Transilvania**, Brașov, România **Teza:** “Advanced Vector Computer Architectures – Specialized Instruction Set Extensions”

Sep 1997 - Iun 2001 **Liceul de Informatică,** Brașov, România

COMPETENTE PERSONALE

Limba maternă: Română

Alte limbi străine cunoscute

	INTELEGERE		VORBIRE		SCRIERE
	Ascultare	Citire	Participare la conversaţie	Discurs oral	
Engleză	C2	C2	C2	C2	C2
Olandeză	A1	A1	A1	A1	A1
Franceză	A1	A1	A1	A1	A1

Competenţe de comunicare
- **Vorbit în public**: prezentări la conferințe, simpozioane
- **Abilități de comunicare scrisă și verbală**: redactarea și prezentarea materialelor la curs și laborator
- **Prezentare și negociere**: prezentarea propunerilor pentru formarea consorțiilor proiectelor europene, negocierea bugetelor proiectelor naționale și europene

Competențe organizaţionale/manageriale
- **Leadership**: Work Package Leader în proiecte europene
- **Bune abilități de management al timpului** deprinse în urma participării în mai multe proiecte europene
- **Gândire critică**: analiza sistemelor complexe și a documentațiilor și identificarea punctelor ce pot fi îmbunătățite

Competenţe dobândite la locul de muncă
- **Lucrul în echipă**: colaborarea cu colegii pentru implementarea proiectelor complexe
- **Aptitudini analitice**: analizarea datelor și informațiilor pentru rezolvarea problemelor complexe
- **Rezolvarea problemelor**: folosirea competențelor pentru a rezolva probleme complexe

Competenţe informatice
- **Programarea Calculatoarelor**: C, C++, CUDA, .NET, C#, Java, FoxPRO, Pascal, Delphi, Bash, Assembly (x86, MIPS, PowerPC, Cell)
- **Design si Verificare de Hardware Digital**: Verilog, System Verilog, VHDL
- **Sisteme de operare**: Linux, Microsoft Windows, MacOS
- **Pachete software specializate**: GCC, Visual Studio, Eclipse, ModelSim, Synplify, Xilinx ISE, Synopsys Design Compiler, Eclipse, Matlab, LaTeX, Microsoft Office, Libre Office, Visio, Photoshop

Permis de conducere
- A, B, C

INFORMATII SUPLIMENTARE

Experiența cu Proiecte Europene de Cercetare

Sep 2015 – Aug 2017 **Co-Principal Investigator, Exploiting eXascale Technology with Reconfigurable Architectures** (EXTRA) project H2020-FETHPC, 4 Milioane de Euro Contribuție UE, www.extrahpc.eu/

Noi 2014 – Apr 2015 **Cercetător PostDoctoral, Green Computing Node for European micro-servers** (EUROSERVER) FP7-ICT, 8.6 Milioane de Euro Contribuție UE, www.euroserver-project.eu/

Noi 2013 – Oct 2014 **Cercetător PostDoctoral, Empowering Young Explorers** (EYE) FP7-ICT, 1.2 Milioane de Euro Contribuție UE, www.fet-eye.eu/

Apr 2012 – Noi 2014 **Cercetător PostDoctoral Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration** (FASTER) FP7-ICT, 2.8 Milioane de Euro Contribuție UE, www.fp7-faster.eu/

Apr 2007 – Dec 2009 **Doctorand**, **Scalable computer ARChitecture** (SARC)
- FP6-IST, 8 Milioane de Euro Contribuție UE, www.sarc-ip.org

Concursuri și Distincții

Sep 2023 **Îndrumătorul echipei de studenți** a Departamentului de Electronică și Calculatoare care a **câștigat concursul AMD/Xilinx Open Hardware cu lucrarea „AI-augumented barcode reader using Xilinx Kria KV260"** la categoria studenți.

Mai 2018	**Best paper award** la Reconfigurable Architectures Workshop, Vancouver, Canada pentru articolul "MAX-PolyMem: High-Bandwidth Polymorphic Parallel Memories for DFEs"
Apr 2007 – Mar 2009	**Netherlands Organization for International Cooperation in Higher Education (Nuffic)** Bursă de 2 ani pentru doctorat acordată studenților internaționali de top care au absolvit Masterul în Olanda
Sep 2005 – Aug 2006	**Bursă UE Socrates, pentru studiul în străinătate** Bursă de 1 an pentru finalizarea lucrării de diplomă la Delft University of Technology, Olanda
Mai 2001	**American Computer Science League (ACSL)** Etapa finală a concursului de programare All-Star Contest, Miami, Florida, SUA

Anexă - Lista Lucrărilor Științifice

Articole în revistă cotată ISI WoS cu SRI > 0.5, ca prim autor

1. **C.B. Ciobanu**, G. Gaydadjiev, C. Pilato and D. Sciuto, The Case for Polymorphic Registers in Dataflow Computing, International Journal of Parallel Programming, December 2018, pp. 1185-1219, https://doi.org/10.1007/s10766-017-0494-1
Online:
https://link.springer.com/article/10.1007/s10766-017-0494-1
SRI: 0.608

Alte articole ISI WoS cu SRI > 0.5

1. A. L. Machidon, O. M. Machidon, **C. B. Ciobanu**, and P. L. Ogrutan, "Accelerating a Geometrical Approximated PCA Algorithm Using AVX2 and CUDA," Remote Sensing, vol. 12, no. 12, p. 1918, Jun. 2020
   https://doi.org/10.3390/rs12121918
Online:
https://www.mdpi.com/2072-4292/12/12/1918/htm
SRI: 4.509 (2019) ; 5-Year Impact Factor: 5.001 (2019)
2. G. Stramondo, **C.B. Ciobanu**, C. de Laat, A.L. Varbanescu, Designing and Building Application-Centric Parallel Memories, in Concurrency and Computation: Practice and Experience, https://doi.org/10.1002/cpe.5485
Online:
https://onlinelibrary.wiley.com/doi/full/10.1002/cpe.5485
SRI: 1.447 (2019), 1.268 (5 year)
3. Pnevmatikatos, K. Papadimitriou, T. Becker, P. Bohm, A. Brokalakis, K. Bruneel, **C.B. Ciobanu**, T. Davidson, G. Gaydadjiev, K. Heyse, W. Luk, X. Niu, I. Papaefstathiou, D. Pau, O. Pell, C. Pilato, M. D. Santambrogio, D. Sciuto, D. Stroobandt, T. Todman, E. Vansteenkiste, FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration, Elsevier Journal on Microprocessors and Microsystems (MICPRO), pp. 321-338, November 2014, ISSN: 0141-9331, eISSN: 1872-9436
   https://doi.org/10.1016/j.micpro.2014.09.006
SRI: 1.161 (2019), 1.119 (5 year)
4. Ramirez, F. Cabarcas, B.H.H. Juurlink, M. Alvarez, F. Sanchez, A. Azevedo, C.H. Meenderinck, **C.B. Ciobanu**, S. Isaza, G. N. Gaydadjiev, The SARC Architecture, IEEE Micro, pp. 16-29, Vol. 30, Nr. 5, ISSN: 0272-1732,
   https://doi.org/10.1109/MM.2010.79
Online:
https://ieeexplore.ieee.org/document/5567090
SRI: 3.172 (2019), 2.682 (5 year) Q1

Alte articole publicate

1. D. Crăciun, N. Bălăceanu, A. Chiriță, **C.B. Ciobanu**, Robotic Arm Control via Hand Movements, International Symposium on Electronics and Telecommunications 2022 (ISETC 2022), pp. 1-4, Timișoara, România, Noiembrie 2022
2. A. Machidon, **C.B. Ciobanu**, O. Machidon, P. Ogrutan, On Parallelizing Geometrical PCA Approximation, 2019 18th RoEduNet Conference: Networking in Education and Research (RoEduNet), pp. 1-6, Galați, România, October 2019, https://doi.org/10.1109/ROEDUNET.2019.8909644
3. L. Stornaiuolo, M. Rabozzi, M. Santambrogio, D. Sciuto, G. Stramondo, **C.B. Ciobanu** and A.L. Varbanescu, HLS Support for Polymorphic Parallel Memories, 26th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI SoC), pp. 143-148, Verona, Italy, October 2018, https://doi.org/10.1109/VLSI-SoC.2018.8644899

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4. G. Stramondo, **C. B. Ciobanu**, A. L. Varbanescu, C. de Laat, Towards Application-Centric Parallel Memories, Euro-Par 2018: Parallel Processing Workshops, pp. 481-493, Turin, Italy, August 2018, https://doi.org/10.1007/978-3-030-10549-5_38
5. **C. B. Ciobanu**, G. Stramondo, A. L. Varbanescu, A. Brokalakis, A. Nikitakis, L. Di Tucci, M. Rabozzi, L. Stornaiuolo, M. Santambrogio, G. Chrysos, C. Vatsolakis, C. Georgios, and D. Pnevmatikatos, EXTRA: An Open Platform for Reconfigurable Architectures, 2018 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS XVIII, pp. 220-229, Samos Island, Greece, July 2018, https://doi.acm.org/10.1145/3229631.3236092
6. **C. B. Ciobanu**, G. Stramondo, C. de Laat and A. L. Varbanescu, MAX-PolyMem: High-Bandwidth Polymorphic Parallel Memories for DFEs, 2018 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), pp. 107-114, Vancouver, Canada, May 2018, https://doi.org/10.1109/IPDPSW.2018.00025
7. Kulkarni, P. Bahrebar, D. Stroobandt, G. Stramondo, **C. B. Ciobanu** and A. L. Varbanescu, A NoC-based Custom FPGA Configuration Memory Architecture for Ultra-fast Micro-reconfiguration, 2017 International Conference on Field Programmable Technology (ICFPT), pp. 203-206, Melbourne, Australia, December 2017, https://doi.org/10.1109/FPT.2017.8280141
8. M. Rabozzi, R. Brondolin, G. Natale, E. Del Sozzo, M. Huebner, A. Brokalakis, **C.B. Ciobanu**, D. Stroobandt, M. Santambrogio, A CAD Open Platform for High Performance Reconfigurable Systems in the EXTRA Project, 2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 368-373, Bochum, Germany, July 2017, https://doi.org/10.1109/ISVLSI.2017.71
9. D. Stroobandt, **C.B. Ciobanu**, M. Santambrogio, G. Figueiredo, A. Brokalakis, D. Pnevmatikatos, M. Huebner, T. Becker, A. Thom., An Open Reconfigurable Research Platform as Stepping Stone to Exascale High-performance Computing, Proceedings of the Conference on Design, Automation & Test in Europe (DATE), pp 416-421, Lausanne, Switzerland, March 2017, https://doi.org/10.23919/DATE.2017.7927026
10. D. Stroobandt, A.L. Varbanescu, **C.B. Ciobanu**, M. Al Kadi, A. Brokalakis, G. Charitopoulos, T. Todman, X. Niu, D. Pnevmatikatos, A. Kulkarni, E. Vansteenkiste, W. Luk, M. Santambrogio, D. Sciuto, M. Huebner, T. Becker, G. Gaydadjiev, A. Nikitakis, A. Thom, EXTRA: Towards the exploitation of eXascale technology for reconfigurable architectures, 2016 11th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), pp. 1-7, Tallinn, June 2016, https://doi.org/10.1109/ReCoSoC.2016.7533896
11. G. Stramondo, A. Varbanescu, **C.B. Ciobanu**, The Case for Custom Parallel Memories: an Application-centric Analysis, Second International Workshop on Heterogeneous High-performance Reconfigurable Computing (H2RC), Salt Lake City, UT, USA, 2016
12. **C.B. Ciobanu,** A. L. Varbanescu, D. Pnevmatikatos, G. Charitopoulos, X. Niu, W. Luk, M. D. Santambrogio, D. Sciuto, M. A. Kadi, M. Huebner, T. Becker, and G. Gaydadjiev, A. Brokalakis, A. Nikitakis, A. J. W. Thom, E. Vansteenkiste, D. Stroobandt, EXTRA: Towards an Efficient Open Platform for Reconfigurable High Performance Computing, 2015 IEEE 18th International Conference on Computational Science and Engineering, pp. 339-342, Porto, Portugal, October 2015, https://doi.org/10.1109/CSE.2015.54
13. G. Smaragdos, C. Davies, C. Strydis, I. Sourdis, **C.B. Ciobanu** , O. Mencer, C. De Zeeuw, Real-Time Olivary Neuron Simulations on Dataflow Computing Machines, Proceedings of International Supercomputing Conference (ISC 2014), pp. 487-497, Leipzig, Germany, June 2014, https://doi.org/10.1007/978-3-319-07518-1_34
14. **C.B. Ciobanu**, G.N. Gaydadjiev, C. Pilato, D. Sciuto, Dataflow Computing with Polymorphic Registers, Proceedings of the 2013 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS 2013), pp. 314-321, Samos, Greece, July 2013, https://doi.org/10.1109/SAMOS.2013.6621140
15. **C.B. Ciobanu**, D.N. Pnevmatikatos, K.D. Papadimitriou, G.N. Gaydadjiev, FASTER Run-time Reconfiguration Management, Proceedings of the 27th International Conference on Supercomputing (ICS 2013), pp. 463-464, Eugene, Oregon, USA, June 2013, https://doi.org/10.1145/2464996.2467283
16. **C.B. Ciobanu**, G. N. Gaydadjiev, Separable 2D Convolution with Polymorphic Register Files, Proceedings of the 2013 Conference on Architecture of Computing Systems (ARCS 2013), pp. 317-328, Prague, Czech Republic, February 2013, https://doi.org/10.1007/978-3-642-36424-2_27
17. K. Papadimitriou, C. Pilato, D. Pnevmatikatos, M.D. Santambrogio, **C.B. Ciobanu**, T. Todman, T. Becker, T. Davidson, X. Niu, G. N. Gaydadjiev, W. Luk, D. Stroobandt, Novel Design Methods and a Tool Flow for Unleashing Dynamic Reconfiguration, Proceedings of the 15 th International Conference on Computational Science and Engineering (CSE 2012), pp. 391-398, December 2012, https://doi.org/10.1109/ICCSE.2012.61
18. **C.B. Ciobanu**, G. Kuzmanov, G. N. Gaydadjiev, Scalability Study of Polymorphic Register Files, Proceedings of the international conference on Digital System Design (DSD 2012), pp. 803-808, Cesme, Izmir, Turkey, September 2012, https://doi.org/10.1109/DSD.2012.116
19. **C.B. Ciobanu**, G. Kuzmanov, G. N. Gaydadjiev, On Implementability of Polymorphic Register Files, Proceedings of the 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC 2012), pp. 1-6, York, UK, July 2012, https://doi.org/10.1109/ReCoSoC.2012.6322873
20. **C. B. Ciobanu**, G. Kuzmanov, A. Ramirez, G. N. Gaydadjiev, Parallel Access Schemes for Polymorphic Register Files: Motivation Study, Advanced Computer Architecture and Compilation for Embedded Systems (ACACES), pp. 127-130, Fiuggi, Italy, 2011
21. **C. B. Ciobanu**, X. Martorell, G. Kuzmanov, A. Ramirez, G. N. Gaydadjiev, Scalability Evaluation of a Polymorphic Register File: a CG Case Study, Proceedings of the 2011 Conference on Architecture of Computing Systems (ARCS 2011), pp. 13-25, Como, Italy, 2011, https://doi.org/10.1007/978-3-642-19137-4_2
22. **C. B. Ciobanu**, G. Kuzmanov, A. Ramirez, G. N. Gaydadjiev, A Polymorphic Register File for Matrix Operations, Proceedings of the 2010 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS 2010), pp. 241-249, Samos, Greece, 2010, https://doi.org/10.1109/ICSAMOS.2010.5642059
23. C. B. Ciobanu, G. Kuzmanov, A. Ramirez, G. N. Gaydadjiev, A Polymorphic Register File Architecture, Advanced Computer Architecture and Compilation for Embedded Systems (ACACES), pp. 245-248, Terrassa, Spain, 2009
24. D. Theodoropoulos, **C. B. Ciobanu**, G. Kuzmanov, Wave Field Synthesis for 3D Audio: Architectural Prospectives, ACM International Conference on Computing Frontiers, pp. 127-136, Ischia, Italy, 2009, https://doi.org/10.1145/1531743.1531764
25. B. Spinean, **C. B. Ciobanu**, G. Kuzmanov, G. N. Gaydadjiev, Design Considerations for a Domain Specific Vector Microarchitecture, in proceedings of PRORISC 2007, pp. pp. 178-184, Veldhoven, The Netherlands, 2007

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26. **C. B. Ciobanu**, B. Spinean, G. Kuzmanov, G. N. Gaydadjiev, Customized Vector Instruction Set Architecture, proceedings of PRORISC 2007, pp. 128-137, Veldhoven, The Netherlands, 2007

Volume de specialitate publicate în edituri recunoscute național

1. **C.B. Ciobanu**, Customizable Register Files for Multidimensional SIMD architectures, Delft University of Technology, 2013, ISBN 978-94-6186-121-4, https://doi.org/10.4233/uuid:6da2ee07-99df-450d-93bd-2367725f4f70
2. L. Stornaiuolo, M. Rabozzi, M. D. Santambrogio, D. Sciuto, **C. B. Ciobanu**, G. Stramondo, A. L. Varbanescu, Building High-Performance, Easy-to-Use Polymorphic Parallel Memories with HLS, capitol în VLSI-SoC: Design and Engineering of Electronics Systems Based on New Computing Paradigms, Springer, Cham, 2019, ISBN 978-3-030-23424-9, https://doi.org/10.1007/978-3-030-23425-6_4
3. **C.B. Ciobanu**, Introducere în Proiectarea Sistemelor Încorporate, Editura Universității Transilvania din Brașov, 2022, ISBN 978-606-19-1564-4

01.10.2023

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